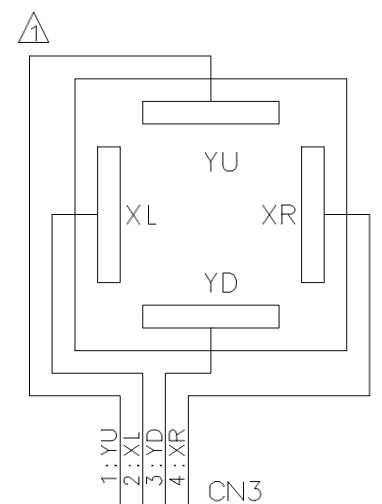
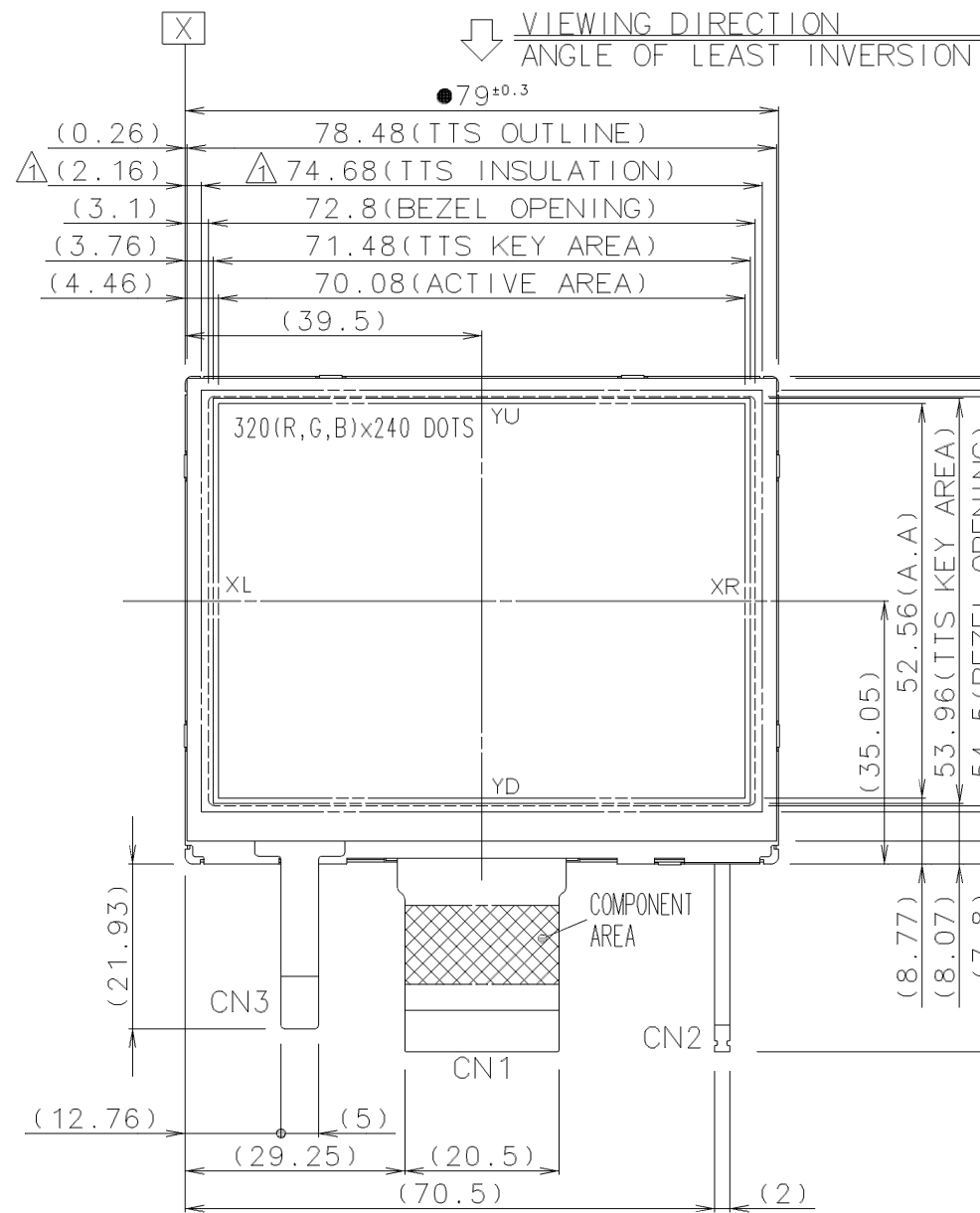
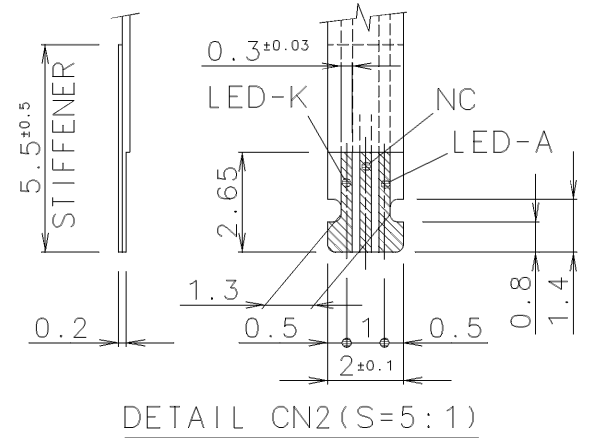


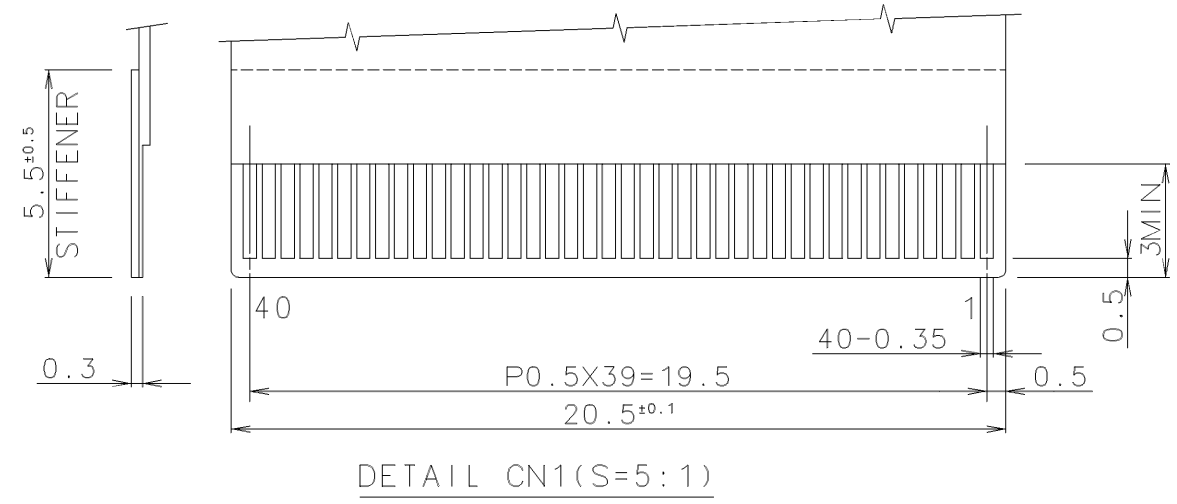


TTS CIRCUIT DIAGRAM

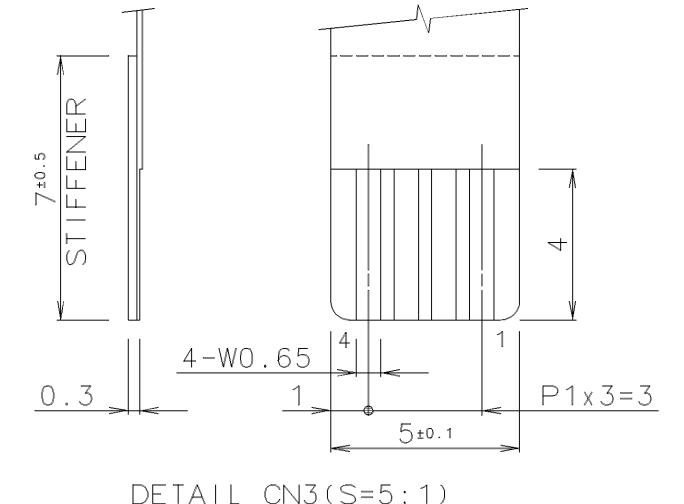


DETAIL CN2 (S=5:1)

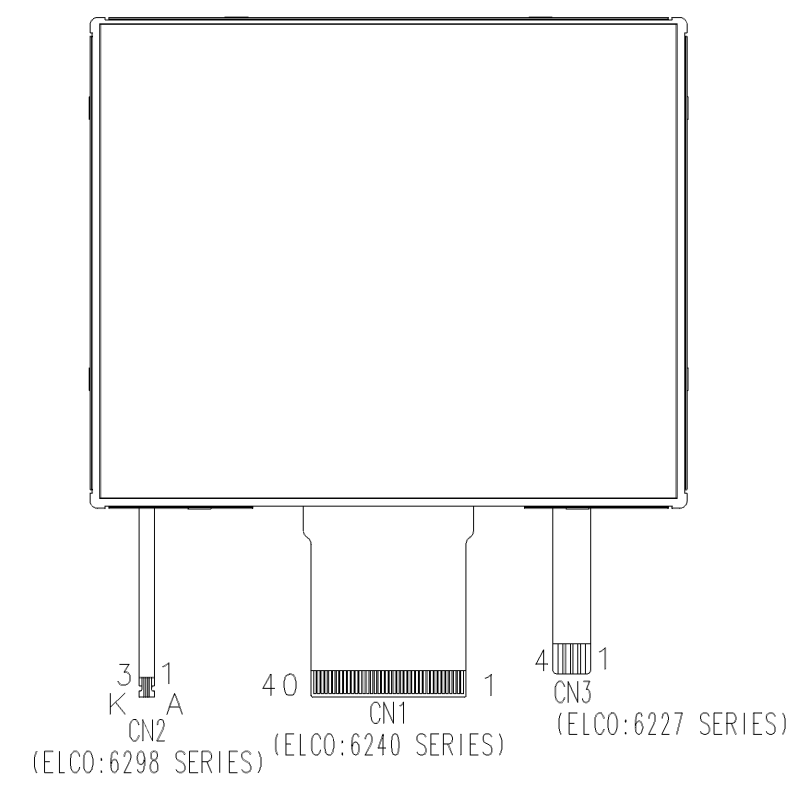
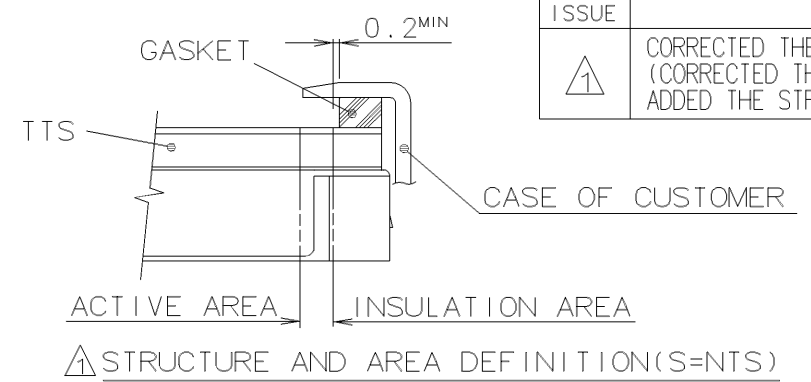
NOTE
THE DIMENSIONS WITH THE MARK (●) ARE CONTROLLED
AS A PARTICULAR CHARACTERISTIC.



DETAIL CN1 (S=5:1)



DETAIL CN3 (S=5:1)



COMPONENT AREA

CONTACT SIDE

1.5 MAX

COMPONENT HIGHT

ISSUE	REVISIONS	DRAWN	DATE
△	CORRECTED THE PIN ASSIGNMENT OF CN3. (CORRECTED THE MISDESCRIPTION) ADDED THE STRUCTURE AND AREA DEFINITION	S. SANO	JUN.24'08

CN1 PIN ASSIGNMENT			
NO.	SYMBOL	NO.	SYMBOL
1	RL	21	DB10
2	TB	22	DB9
3	DOTCLK	23	DB8
4	VSYNC	24	GND
5	HSYNC	25	DB7
6	ENABLE	26	DB6
7	DB23	27	DB5
8	DB22	28	DB4
9	DB21	29	DB3
10	DB20	30	DB2
11	DB19	31	DB1
12	DB18	32	DB0
13	DB17	33	SDI
14	DB16	34	SCL
15	GND	35	CS
16	DB15	36	RESET
17	DB14	37	SDO
18	DB13	38	GND
19	DB12	39	VCC
20	DB11	40	VCC

CN2 PIN ASSIGNMENT			
NO.	SYMBOL	NO.	SYMBOL
1	LED-A	3	LED-K
2	NC		

CN3 PIN ASSIGNMENT			
NO.	SYMBOL	NO.	SYMBOL
1	YU	3	YD
2	XL	4	XR

TOLERANCE				MATERIAL:		FINISH:	
MEASURE	A	B	C	DATE	THIRD ANGLE PROJECTION	OPTREX CORPORATION	
L≤16	±0.1	±0.3	±1	2008/06/26	SCALE UNIT		
16<L≤63	±0.2	±0.5	±1.5	APPROVED	1:1 mm	TITLE	
63<L≤250	±0.3	±0.8	±2	Noboru Wada	DATE APR.22'08	DIMENSIONAL OUTLINE	
250<L≤500	±0.5	±1.2	±3	CHECKED		DWG NO(CODE)	
500<L	±0.8	±2	±4	Yasuo Yamaguchi		T-55343AE BASE	
ANGLE	±1°	±5°	±10°	DRAWN	DSGN	DWG SIZE	
				Satoshi Sano	S. Sano	A3	
						DWG REV	
						A	