# Specification





| Written by Department | Written by / Date | Approved by QRA Manager | Issued by D.C.C. |
|---|---|---|---|
| Research & Development | Charlie Cheng<br>11/25/2003 | Joey Hsiao<br>12/08/2003 | Kuo-wei Lee<br>12/08/2003 |

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| Code Name | 100 | 200 | 300 | 400 | 500 | 600 | 700 |
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| Dept. | HR | S/M | MFG | R&D | CH | QRA | MIS |
| | -- | -- | -- | ✓ | ✓ | ✓ | -- |

## 文件變更履歷頁

## Document Change History

| 版次 Rev. | 變更項次 Change Items# | 變更內容簡述 Change Description | 變更依據文件號碼 ECN # | 生效日期 Eff. Date |
|---|---|---|---|---|
| 001 | -- | New Release | E11030004 | 12/08/2003 |
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# IST3028 120-output LCD Common Gate Driver IC

## DESCRIPTION

The IST3028 is a 120-output common gate driver IC and suitable for driving medium/large size dot matrix LCD panels. The IST3028 provides function for both single and dual mode operations, also suitable for a low power consumption, and high-precision LCD.



## FEATURES

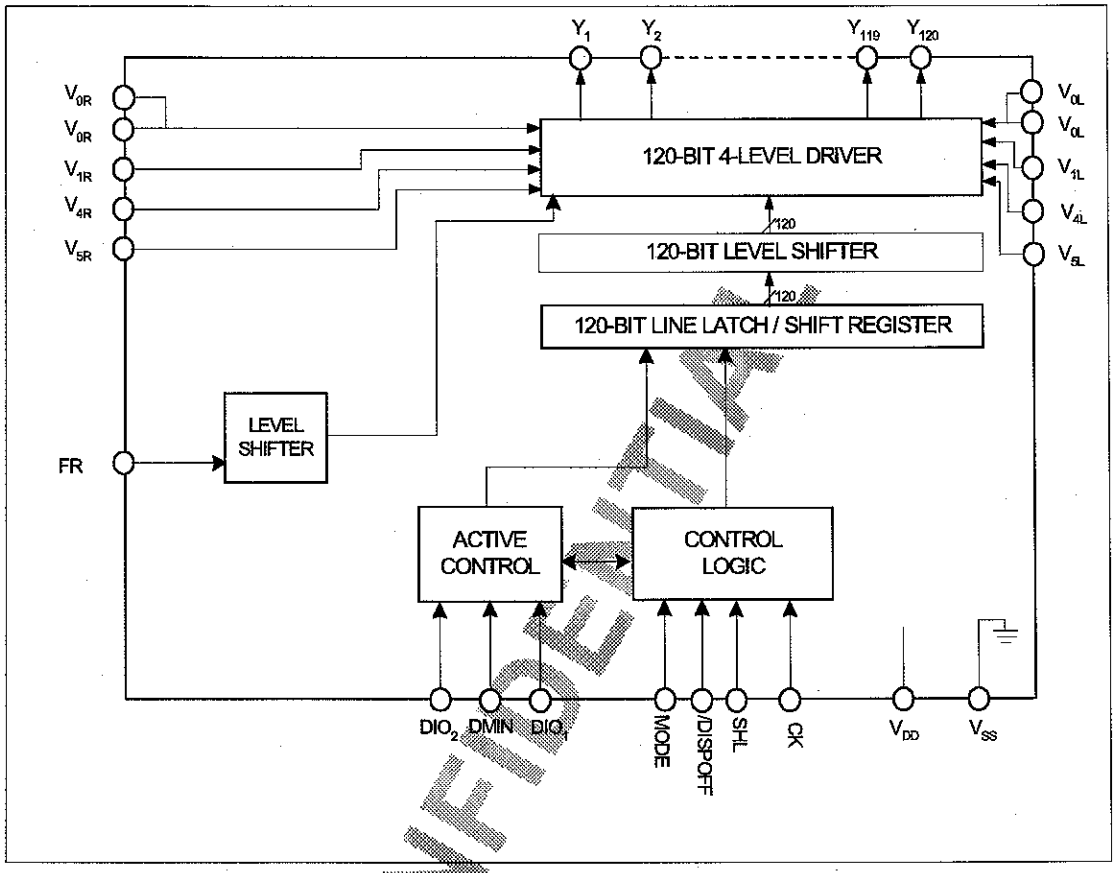
- Number of LCD drive outputs: 120
- Supply voltage for the logic system: +2.5 to +5.5 V
- Supply voltage for LCD drive: +10.0 to + 40.0 V
- Low power consumption
- Low output impedance
- Operating temperature: -20 to +85℃
- Shift clock frequency : 4 MHz(MAX.)
- Built-in 120-bit bi-directional shift register (Divisible by 60 bits x 2)
- Available in a single mode (120-bit shift register) or in a dual mode(60-bit shift register x 2)

(1) $Y_1 \rightarrow Y_{120}$ Single mode
(2) $Y_{120} \rightarrow Y_1$ Single mode
(3) $Y_1 \rightarrow Y_{60}$, $Y_{61} \rightarrow Y_{120}$ Dual mode
(4) $Y_{120} \rightarrow Y_{61}$, $Y_{60} \rightarrow Y_1$ Dual mode

- Shift register circuits may reset by active /DISPOFF

Package : TCP/Gold Bumped Chip

**BLOCK DIAGRAM**



## BASIC OPERATIONS AND DESCRIPTION OF FUNCTION BLOCKS

| BLOCK | FUNCTION |
|---|---|
| Active Control | Depending on the master/slave, single/dual mode and left/right shift direction of the device, Active Control module determines the function of DIO1/DIO2 and DMIN as an input or output signal interface. Once the completion to shift 120-bit channels, the active device becomes non-active, then cascades a signal through DIO1/DIO2 to active next device. |
| Control Logic | With the input signals of MODE, SHL, and CK, the Control Logic will determine the direction to shift data pulse. |
| Line Latch/ Shift Register | Shift data from DIO1/DIO2 and DMIN to DIO2/DIO1. Data shift at falling edge of CK clock. |
| Level Shifter | Level Shifter changes signal voltage up to LCD output voltage level. |
| 4-Level Driver | There are four different voltages connect to the block, and only one of the voltages is driven to the output at a time. This block is a voltage selector, and the selection is based on FR, and /DISPOFF setting. |

## PIN DESCRIPTION

| SYMBOL | I/O | DESCRIPTION |
|---|---|---|
| $Y_1 \rightarrow Y_{120}$ | O | LCD drive output |
| $V_{0L}$, $V_{0R}$ | - | Power supply for LCD drive |
| $V_{1L}$, $V_{1R}$ | - | Power supply for LCD drive |
| $V_{4L}$, $V_{4R}$ | - | Power supply for LCD drive |
| $V_{5L}$, $V_{5R}$ | - | Power supply for LCD drive |
| SHL | I | Left or Right shift direction selection control pin |
| $V_{DD}$ | - | Power supply for logic system (+2.5 to +5.5 V) |
| $DIO_2$, $DIO_1$ | I/O | Input/output pin for input data initialization/completion of IST3028. Please refer to Function Description for detail function definition. |
| DMIN | I | Dual mode data input for Common mode operation |
| /DISPOFF | I | LCD driver output control disable pin |
| CK | I | Clock for chip device use |
| FR | I | Polarity switch control pin |
| MODE | I | Mode selection control pin, 4-bit/8-bit mode at Segment, single/dual data mode at Common. |
| $V_{SS}$ | - | Ground (0 V) |

## FUNCTIONAL DESCRIPTION

### Pin Functions

| SYMBOL | FUNCTION |
|---|---|
| $V_{DD}$ | Logic system power supply pin, connected to +2.5 to +5.5 V. |
| $V_{SS}$ | Ground pin, connected to 0 V. |
| $V_{0L}$, $V_{0R}$<br>$V_{1L}$, $V_{1R}$<br>$V_{4L}$, $V_{4R}$<br>$V_{5L}$, $V_{5R}$ | Biased power supply pins for LCD driver voltage<br>• Normally the biased voltages is set by a resistor divider<br>• Ensure the voltages are set such that $V_{SS} \leq V_5 < V_4 \leq V_1 < V_0$. |
| $DIO_1$ ~$DIO_2$ | Input/output pin for initialization/completion of IST3028.<br>**At single mode**<br>• If SHL sets to $V_{SS}$ level "L", $DIO_1$ is input and $DIO_2$ is output.<br>• If SHL sets to $V_{DD}$ level "H", $DIO_2$ is input and $DIO_1$ is output.<br>**At dual mode:**<br>• If SHL sets to $V_{SS}$ level "L", both $DIO_1$ and DMIN are input and $DIO_2$ is output.<br>• If SHL sets to $V_{DD}$ level "H", both $DIO_2$ and DMIN are input and $DIO_1$ is output.<br>• Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations. |
| CK | Shift clock pulse input pin for bi-directional shift register<br>• Data is shifted at the falling edge of the clock pulse. |
| SHL | Left or Right shift direction control selection pin<br>• When SHL set to $V_{SS}$ level "L", IST3028 LCD output is from $Y_1$ to $Y_{120}$ sequentially.<br>• When SHL set to $V_{DD}$ level "H", IST3028 LCD output is from $Y_{120}$ to $Y_1$ sequentially.<br>• Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations. |
| /DISPOFF | LCD driver output control disable pin<br>• When set to $V_{SS}$ level "L", all the LCD driver output pins ($Y_1$-$Y_{120}$) are set to level $V_5$.<br>• This pin also works as a reset function control, and content inside display register will be clear out.<br>• The table of logic values is shown in "**TRUTH TABLE**" in Functional Operations. |

| SYMBOL | FUNCTION |
|---|---|
| FR | Polarity switch control signal<br>• Normally, the polarity changes once at every frame.<br>• Please refer the "**TRUTH TABLE**" in Functional Operations. |
| MODE | Mode selection pin<br>• When set to $V_{SS}$ level "L", single mode is selected;<br>When set to $V_{DD}$ level "H", dual mode is selected.<br>• Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations. |
| DMIN | Dual mode data input pin<br>• If MODE sets to $V_{DD}$ level "H", IST3028 is in the dual mode, and DMIN is the dual mode data input pin.<br>• Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations. |
| $Y_1$-$Y_{120}$ | LCD drive output pins<br>• One of the voltages ($V_0$, $V_1$, $V_4$, or $V_5$) will be driven out to the LCD output. Please refer to the "**TRUTH TABLE**" in Functional Operations. |

**Functional Operations**

**TRUTH TABLE**

| FR | LATCH DATA | /DISPOFF | LCD DRIVE OUTPUT VOLTAGE LEVEL ($Y_1$-$Y_{120}$) |
|---|---|---|---|
| L | L | H | $V_4$ |
| L | H | H | $V_0$ |
| H | L | H | $V_1$ |
| H | H | H | $V_5$ |
| X | X | L | $V_5$ |

**NOTES:**

- $V_{SS} \leq V_5 < V_4 < V_1 < V_0$, L: $V_{SS}$ (0 V), H: $V_{DD}$ (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supplied regular voltages are assigned by specification for each power pin.



**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**

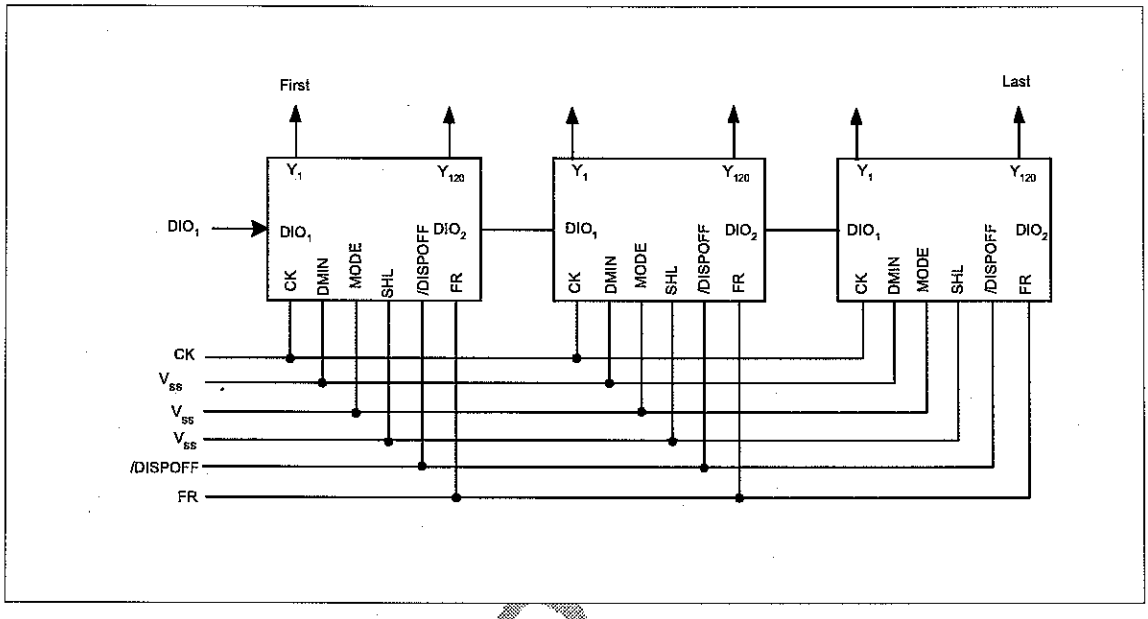
| MODE | SHL | DATA TRANSFER DIRECTION | $DIO_1$ | $DIO_2$ | DMIN |
|---|---|---|---|---|---|
| L (Single) | L | $Y_1 \rightarrow Y_{120}$ | Input | Output | X |
| | H | $Y_{120} \rightarrow Y_1$ | Output | Input | X |
| H (Dual) | L | $Y_1 \rightarrow Y_{60}$<br>$Y_{61} \rightarrow Y_{120}$ | Input | Output | Input |
| | H | $Y_{120} \rightarrow Y_{61}$<br>$Y_{60} \rightarrow Y_1$ | Output | Input | Input |

**NOTES:**

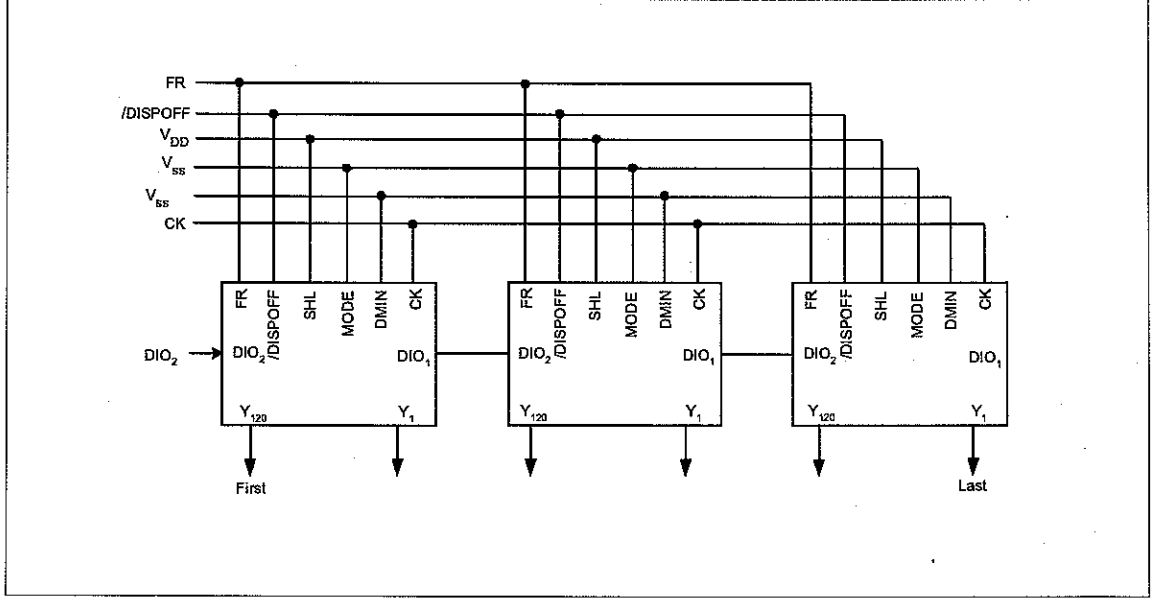
- L: $V_{SS}$ (0 V), H: VDD (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

## CONNECTION EXAMPLES FOR MULTIPLE COMMON DRIVERS

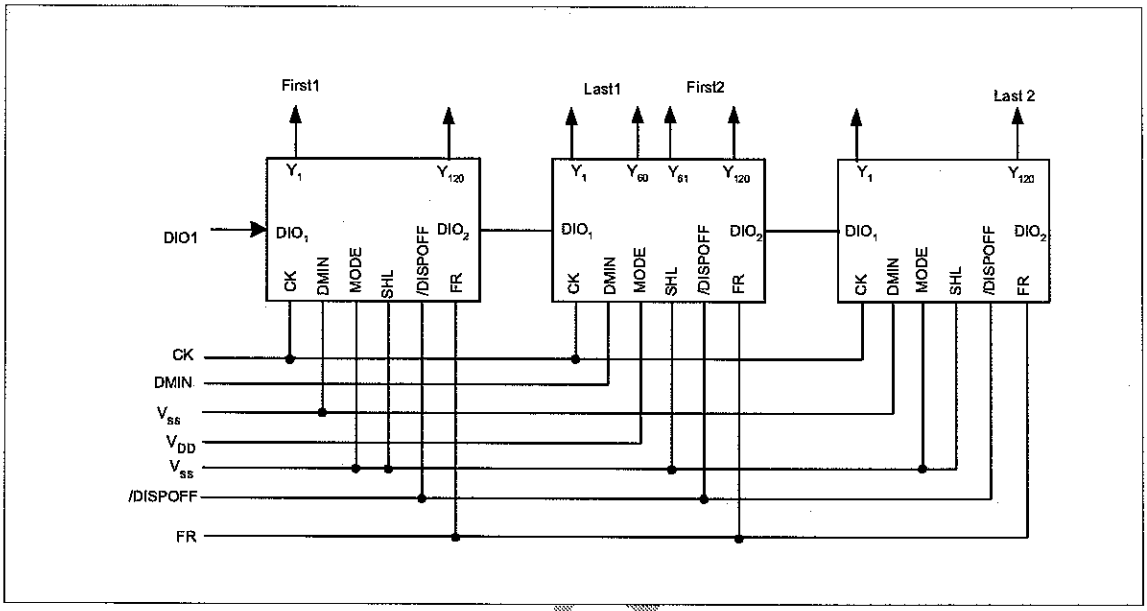
### (a) Single Mode (SHL= "L")



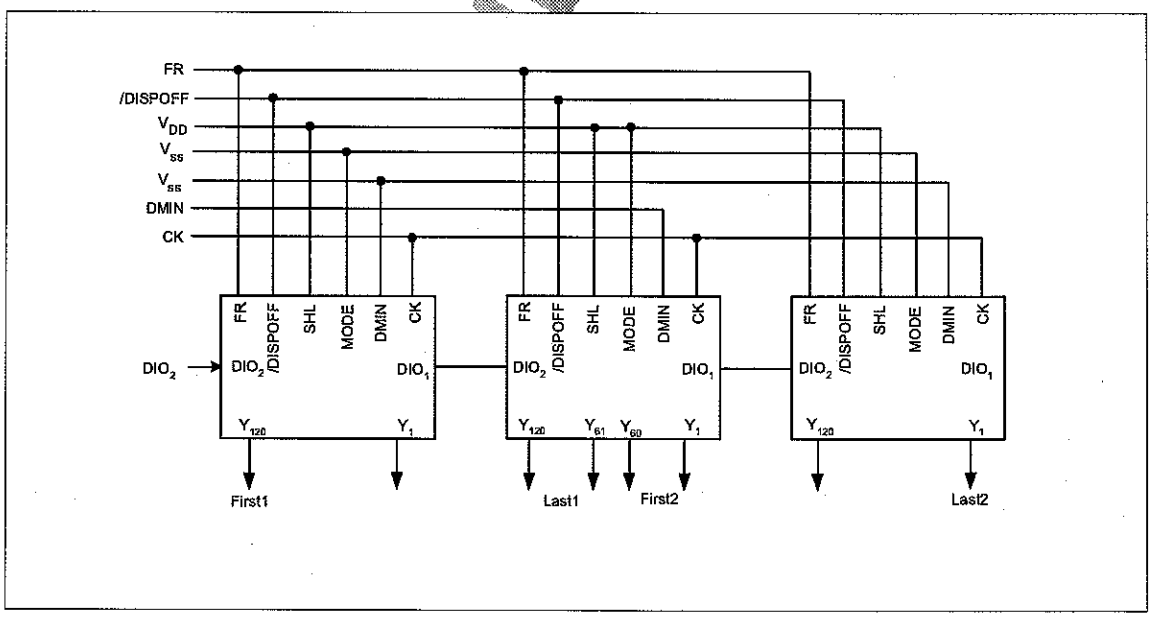

### (b) Single Mode (SHL= "H")



**(c) Dual Mode (SHL= "L")**




**(d) Dual Mode (SHL= "H")**



**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER | SYMBOL | APPLICABLE PINS | RATING | UNIT | NOTE |
|---|---|---|---|---|---|
| Supply voltage (1) | $V_{DD}$ | $V_{DD}$ | -0.3 to +7.0 | V | 1,2 |
| Supply voltage (2) | $V_0$ | $V_{0L}$, $V_{0R}$ | -0.3 to +45.0 | V | |
| | $V_1$ | $V_{1L}$, $V_{1R}$ | -0.3 to V0 +0.3 | V | |
| | $V_4$ | $V_{4L}$, $V_{4R}$ | -0.3 to V0 +0.3 | V | |
| | $V_5$ | $V_{5L}$, $V_{5R}$ | -0.3 to V0 +0.3 | V | |
| Input voltage | $V_I$ | CK, MODE, FR, SHL, $DIO_1$, $DIO_2$, /DISPOFF, DMIN | -0.3 to VDD +0.3 | V | |
| Storage temperature | $T_{STG}$ | | -45 to +125 | ℃ | |

**NOTES:**

1. TA= +25 ℃

2. The maximum applicable voltage on any pin with respect to $V_{SS}$ (0 V).

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Supply voltage (1) | $V_{DD}$ | $V_{DD}$ | +2.5 | | +5.5 | V | 1,2 |
| Supply voltage (2) | $V_0$ | $V_{0L}$, $V_{0R}$ | +15.0 | | +42.0 | V | |
| Operating temperature | $T_{OPR}$ | | -20 | | +85 | ℃ | |

**NOTES:**

1. The applicable voltage on any pin with respect to $V_{SS}$ (0 V).

2. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_4 < V_1 < V_0$.

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{SS}$= $V_5$= 0 V, $V_{DD}$= +2.5 to +5.5 V, $V_0$= +15.0 to +42.0 V, $T_{OPR}$= -20 to +85 ℃)

| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | $DIO_1$, $DIO_2$, CK, DMIN SHL, MODE, FR /DISPOFF | | | $0.2V_{DD}$ | V | |
| Input "High" voltage | $V_{IH}$ | | | $0.8V_{DD}$ | | | V | |
| Output "Low" voltage | $V_{OL}$ | $I_{OL}$=+0.4 mA | $DIO_1$, $DIO_2$ | | | +0.4 | V | |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$=-0.4 mA | | $V_{DD}$-0.4 | | | V | |
| Input leakage current | $I_{LIL}$ | $V_I = V_{SS}$ | $DIO_1$, $DIO_2$, CK, DMIN SHL, MODE, FR /DISPOFF | | | -10.0 | μA | |
| | $I_{LIH}$ | $V_I = V_{DD}$ | CK, SHL, MODE, FR /DISPOFF | | | +10.0 | μA | |
| Input pull-down current | $I_{PD}$ | $V_I = V_{DD}$ | DMIN, $DIO_1$, $DIO_2$ | | | 100.0 | μA | |
| Output resistance | $R_{ON}$ | $\lvert\Delta V_{ON}\rvert$ =0.5V, $V_0$=40V | $Y_1$-$Y_{120}$ | | 0.5 | 0.8 | KΩ | |
| | | $\lvert\Delta V_{ON}\rvert$ =0.5V, $V_0$=30V | | | 0.8 | 1.3 | | |
| | | $\lvert\Delta V_{ON}\rvert$ =0.5V, $V_0$=20V | | | 1.3 | 1.8 | | |
| Standby current | $I_{STB}$ | | $V_{SS}$ | | | 50.0 | μA | 1 |
| Supply current (1) | $I_{DD}$ | | $V_{DD}$ | | | 60.0 | μA | 2 |
| Supply current (2) | $I_0$ | | $V_{0L}$, $V_{0R}$ | | | 120.0 | μA | 2 |



**NOTES:**

1. $V_{DD}$ = +5.0 V, $V_0$ = +42.0 V, $V_I$ = $V_{SS}$

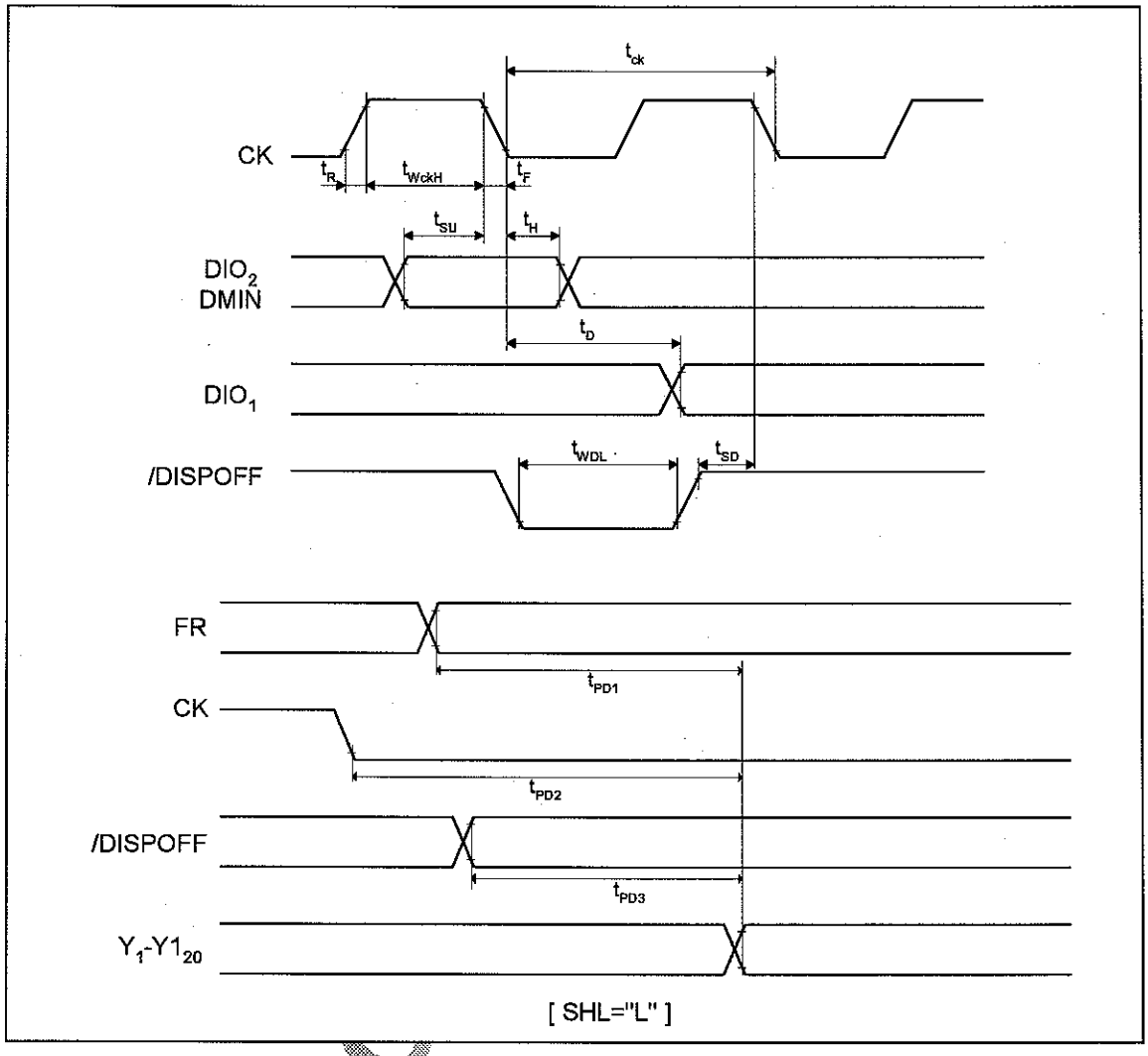
2. $V_{DD}$ = +5.0 V, $V_0$ = +42.0 V, $f_{CK}$ = 41.6 kHz, $f_{FR}$ = 80 Hz, 1/480 duty operation, no-load.

**AC Characteristics**

($V_{SS}$ = $V_5$ = 0 V, $V_{DD}$ = +2.5 to +5.5 V, $V_0$ = +15.0 to +42.0 V, $T_{OPR}$ = -30 to +85 ℃)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Shift clock period | $t_{CK}$ | $V_{DD}$ = +5.0 ± 0.5V | 250 | | | ns |
| | | $V_{DD}$ = +2.5 to + 4.5V | 330 | | | |
| Shift clock "H" pulse width | $t_{WCKH}$ | $V_{DD}$ = +5.0 ± 0.5V | 15 | | | ns |
| | | $V_{DD}$ = +2.5 to + 4.5V | 30 | | | ns |
| Data setup time | $t_{SU}$ | | 30 | | | ns |
| Data hold time | $t_H$ | | 50 | | | ns |
| Input signal rise time | $t_R$ | | | | 50 | ns |
| Input signal fall time | $t_F$ | | | | 50 | ns |
| /DISPOFF removal time | $t_{SD}$ | | 100 | | | ns |
| /DISPOFF "L" pulse width | $T_{WDL}$ | | 1.2 | | | µs |
| Output delay time (1) | $t_D$ | $C_L$ = 15 pF<br>$V_{DD}$ = +5.0 ± 0.5V | | | 170 | ns |
| | | $C_L$ = 15 pF<br>$V_{DD}$ = +2.5 to + 4.5V | | | 250 | |
| Output delay time (2) | $t_{PD1}$, $t_{PD2}$ | $C_L$ = 15 pF | | | 1.2 | µs |
| Output delay time (3) | $t_{PD3}$ | $C_L$ = 15 pF | | | 1.2 | µs |

**Timing Chart of Common Mode**




[ SHL="L" ]

## PRECAUTIONS

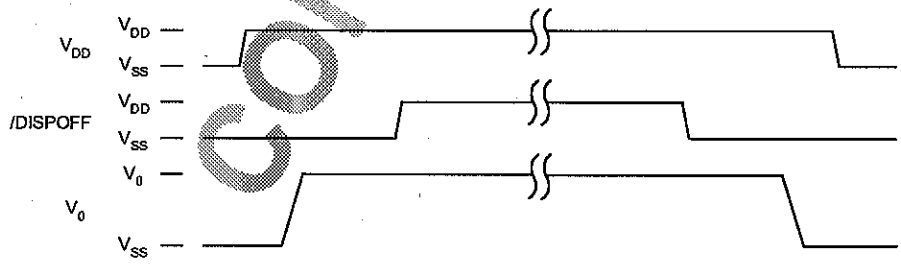
**Precautions when connecting or disconnecting the power supply**

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω ) or fuse to the LCD drive power $V_0$ of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level $V_5$ on /DISPOFF function. Then, disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



# Specification



| Written by Department | Written by / Date | Approved by QRA Manager | Issued by D.C.C. |
|---|---|---|---|
| Research & Development | Charlie Cheng 11/25/2003 | Joey Hsiao 12/08/2003 | Kuo-wei Lee 12/08/2003 |

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| Dept. | HR | S/M | MFG | R&D | CH | QRA | MIS |
| | -- | -- | -- | ✓ | ✓ | ✓ | -- |

文件變更履歷頁

Document Change History

| 版次<br>Rev. | 變更項次<br>Change Items# | 變更內容簡述<br>Change Description | 變更依據文件號碼<br>ECN # | 生效日期<br>Eff. Date |
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| 001 | -- | New Release | E11030004 | 12/08/2003 |
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# IST3029 240-output LCD Segment Gate Driver IC

## DESCRIPTION

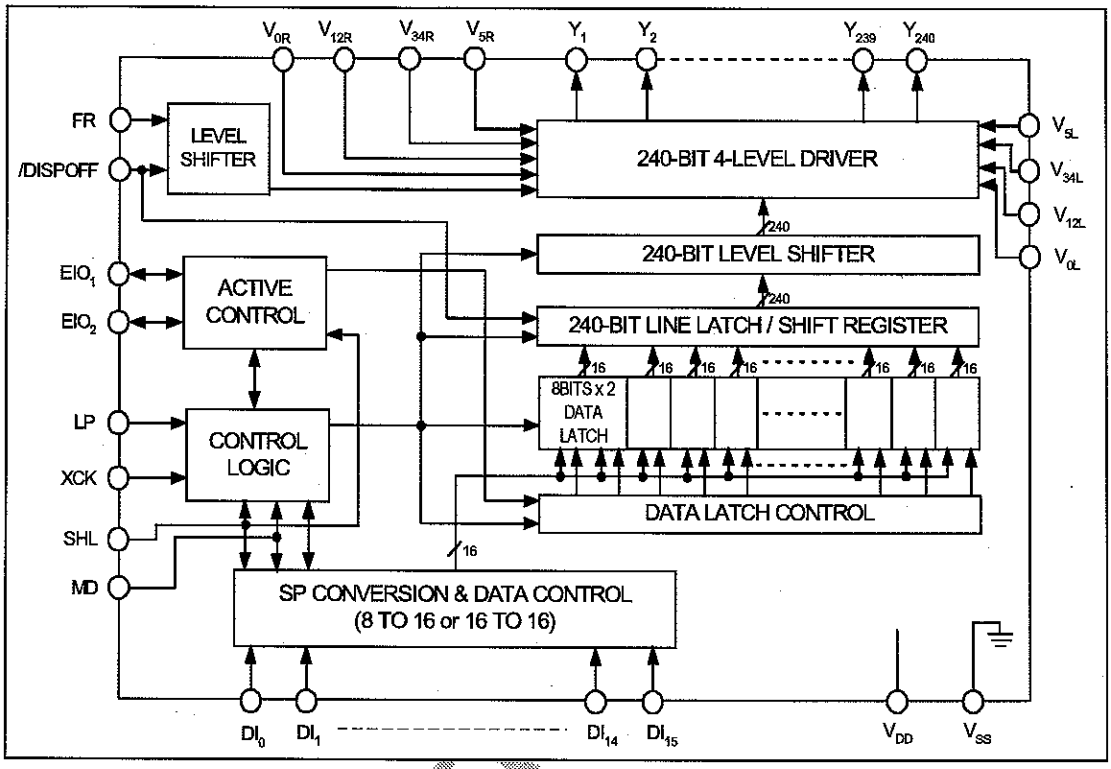
The IST3029 is a 240-output segment gate driver IC and suitable for driving medium/large size dot matrix LCD panels. Also, the IST3029 may use with IST3028 common gate driver, and the combination of these two devices make suitable for a low power consumption, and high-precision LCD product.



## FEATURES

- Number of LCD drive outputs: 240
- Supply voltage for the logic system: +2.5 to +5.5 V
- Supply voltage for LCD drive: +10.0 to + 42.0 V
- Low power consumption
- Low output impedance
- Operating temperature: -20 to +85℃
- Shift clock frequency :
  - 25 MHz (MAX.): $V_{DD}$ = +5.0 to ± 0.5V
  - 15 MHz (MAX.): $V_{DD}$ = +3.0 to + 4.5V
  - 12 MHz (MAX.): $V_{DD}$ = +2.5 to + 3.0V
- Selectable 8-bit/16-bit parallel data bus input
- Built-in 240-bit bi-directional shift register
- Build-in counter stops internal clock at the time of 240 bi-directional registers are full, and may reset automatically with LP signal.
- Shift register circuits may reset by active /DISPOFF
- Package: TCP/Gold Bumped Chip

**BLOCK DIAGRAM**



**BASIC OPERATIONS AND DESCRIPTION OF FUNCTION BLOCKS**

| BLOCK | FUNCTION |
|---|---|
| Active Control | Depending on the master/slave mode and shift direction of the device, Active Control module determines the function of EIO1/EIO2 as an input or output signal pin. Once the completion of 240-bit data latch finished, the active device becomes non-active, then cascades a signal through EIO1/EIO2 to active next device. |
| SP Conversion & Data Control | Control of data $DI_0$~$DI_{15}$ input sequence and organization to pipe data are the major purpose of the block. The pin of MD controls the 16-bit/8-bit data bus input operations. |
| Data Latch Control | Data Latch Control module cascades $DI_0$~$DI_{15}$ input data to the internal data bus also prepares for the 240 data registers to latch. |
| Data Latch | The Data Latch modules take all the 240 data and ready for registers to latch. |
| Line Latch/ Shift Register | The registers in this block stable the date and drive LCD output. The amount of the registers in the module is 240. During Segment mode function, an LP signal will move all the 240 data into register and drive to output. |
| Level Shifter | The major purpose of the Level Shifter is to move the regular logic level to the proper LCD high voltage level. |
| 4-Level Driver | There are four different voltages connect to the block, and only one of the voltages is driven to the output at a time. This block is a voltage selector, and the selection is based on FR, and /DISPOFF setting. |
| Control Logic | The Control Logic module is the most important block of the device. Most control signals connect to this block and determine the operation of the driver. Please refer to Pin Function Description to get detail and idea of the module. |

**PIN DESCRIPTION**

| SYMBOL | I/O | DESCRIPTION |
|---|---|---|
| $Y_1 \rightarrow Y_{240}$ | O | LCD drive output |
| $V_{0L}$, $V_{0R}$ | - | Power supply for LCD drive |
| $V_{12L}$, $V_{12R}$ | - | Power supply for LCD drive |
| $V_{34L}$, $V_{34R}$ | - | Power supply for LCD drive |
| $V_{5L}$, $V_{5R}$ | - | Power supply for LCD drive |
| SHL | I | Left or Right shift direction selection control pin |
| $V_{DD}$ | - | Power supply for logic system (+2.5 to +5.5 V) |
| $EIO_2$, $EIO_1$ | I/O | Input/output pin for input data initialization/completion of the device. Please refer to Function Description for detail function definition. |
| $DI_0$~$DI_{15}$ | I | 8-bit/16-bit parallel data input bus. |
| /DISPOFF | I | LCD driver output control disable pin |
| XCK | I | Clock for chip device use |
| LP | I | Clock for chip device use |
| FR | I | Polarity switch control pin |
| MD | I | Mode selection control pin, 8-bit/16-bit mode selection. |
| $V_{SS}$ | - | Ground (0 V) |

## FUNCTIONAL DESCRIPTION

### Pin Functions

| SYMBOL | FUNCTION |
|---|---|
| $V_{DD}$ | System power supply pin, logic high, connected to +2.5 to +5.5 V. |
| $V_{SS}$ | Ground pin, logic low, connected to 0V. |
| $V_{0L}$, $V_{0R}$<br>$V_{12L}$, $V_{12R}$<br>$V_{34L}$, $V_{34R}$<br>$V_{5L}$, $V_{5R}$ | Biased power supply pins for LCD driver voltage<br>• Normally the biased voltages is set by a resistor divider<br>• Ensure the voltages are set such that $V_{SS} \leq V_5 < V_{34} < V_{12} < V_0$. |
| $DI_0$-$DI_{15}$ | LCD display data input pins<br>• 16-bit/8-bit parallel data input bus.<br>• Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations. |
| XCK | Segment clock input pin for taking display data<br>• Data is read at the falling edge of the clock pulse. |
| LP | Control pin for latching 240 display data<br>• Data is latched at the falling edge of the clock pulse when 240 data input completed. |
| SHL | Left or Right shift direction control selection pin<br>• When SHL set to $V_{SS}$ level "L", IST3029 LCD output is from $Y_{240}$ to $Y_1$.<br>• When SHL set to $V_{DD}$ level "H", IST3029 LCD output is from $Y_1$ to $Y_{240}$.<br>• Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations. |
| /DISPOFF | LCD driver output control disable pin<br>• When set to $V_{SS}$ level "L", all the LCD driver output pins ($Y_1$-$Y_{240}$) are set to level $V_5$.<br>• This pin also works as a reset function control, and content inside the display registers will be clear out.<br>• The table of logic values is shown in "**TRUTH TABLE**" in Functional Operations. |

| SYMBOL | FUNCTION |
|---|---|
| FR | Polarity switch control signal<br>• Please refer the **"TRUTH TABLE"** in Functional Operations. |
| MD | Mode selection pin<br>• When set to $V_{SS}$ level "L", 8-bit parallel input mode is set.<br>• When set to $V_{DD}$ level "H", 16-bit parallel input mode is set.<br>• Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations. |
| $EIO_1$-$EIO_2$ | Input/output pin for initialization/completion of IST3029.<br>**IST3029 as a master device:**<br>As a master device, the $EIO_x$ input pin must connect to Vss. Once a high pulse LP signal comes, an internal counter will reset to zero, and immediately IST3029 is in active mode to take $DI_0$-$DI_7$ or $DI_0$-$DI_{15}$ data. At completion of taking the 240 data, $EIO_x$ output pin sends out a low pulse to active next slave device.<br>• If SHL control pin is at $V_{SS}$ level "L", then $EIO_2$ connects to Vss or 0v, and $EIO_1$ is output.<br>• If SHL control pin is at $V_{DD}$ level "H", then $EIO_1$ connects to Vss or 0v, and $EIO_2$ is output.<br>• Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations.<br><br>**IST3029 as a slave device:**<br>A high pulse LP signal will reset an internal counter of the slave device, and immediately a low pulse sends to $EIO_x$ input pin will active the slave device to take $DI_0$-$DI_7$ or $DI_0$-$DI_{15}$ data. At completion of taking the 240 data, $EIO_x$ output pin sends out a low pulse to active next slave device.<br>• If SHL control pin is at $V_{SS}$ level "L", then $EIO_1$ is output and $EIO_2$ is input.<br>• If SHL control pin is at $V_{DD}$ level "H", then $EIO_1$ is input and $EIO_2$ is output.<br>• Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations. |
| $Y_1$-$Y_{240}$ | LCD drive output pins<br>• One of the voltages ($V_0$, $V_{12}$, $V_{34}$, or $V_5$) will be driven out to the LCD output. Please refer to the **"TRUTH TABLE"** in Functional Operations. |

**Functional Operations**

**TRUTH TABLE**

| FR | LATCH DATA | /DISPOFF | LCD DRIVE OUTPUT VOLTAGE LEVEL ($Y_1$-$Y_{240}$) |
|---|---|---|---|
| L | L | H | $V_{34}$ |
| L | H | H | $V_5$ |
| H | L | H | $V_{12}$ |
| H | H | H | $V_0$ |
| X | X | L | $V_5$ |

**NOTES:**

- $V_{SS} \leq V_5 < V_{34} < V_{12} < V_0$, L: $V_{SS}$ (0 V), H: $V_{DD}$ (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supplied regular voltages are assigned by specification for each power pin.

## RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(a) 8-bit Parallel Input Mode

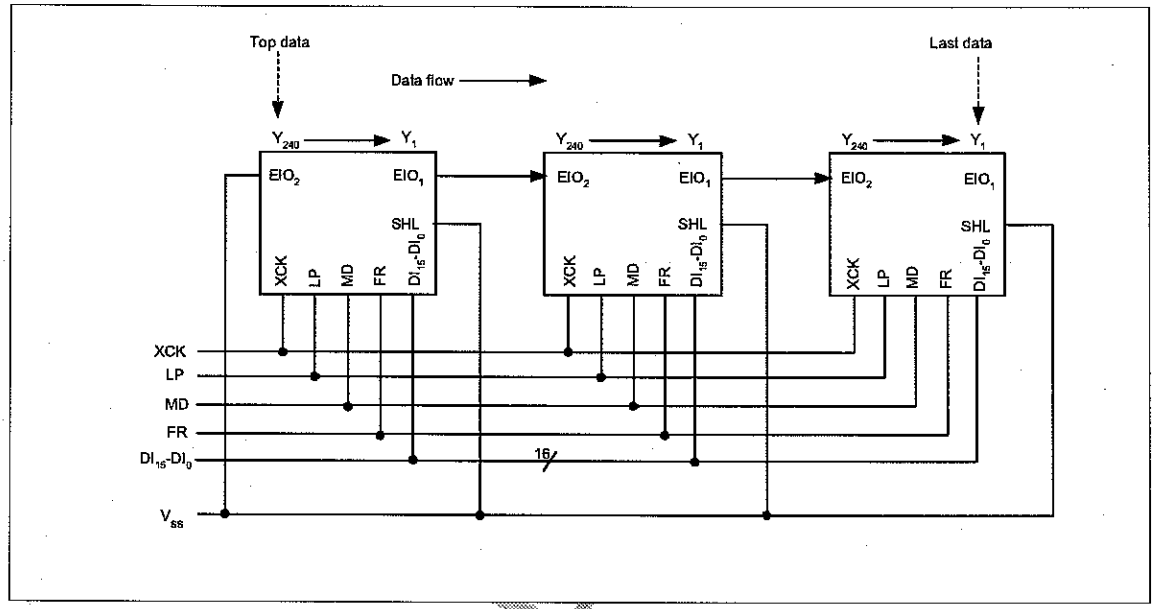
| MD | SHL | $EIO_1$ | $EIO_2$ | DATA INPUT | NUMBER OF CLOCKS | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 30 CLOCK | 29 CLOCK | 28 CLOCK | ... | 3 CLOCK | 2 CLOCK | 1 CLOCK |
| L | L | Output | Input | $DI_0$ | $Y_1$ | $Y_9$ | $Y_{17}$ | ... | $Y_{217}$ | $Y_{225}$ | $Y_{233}$ |
| | | | | $DI_1$ | $Y_2$ | $Y_{10}$ | $Y_{18}$ | ... | $Y_{218}$ | $Y_{226}$ | $Y_{234}$ |
| | | | | $DI_2$ | $Y_3$ | $Y_{11}$ | $Y_{19}$ | ... | $Y_{219}$ | $Y_{227}$ | $Y_{235}$ |
| | | | | $DI_3$ | $Y_4$ | $Y_{12}$ | $Y_{20}$ | ... | $Y_{220}$ | $Y_{228}$ | $Y_{236}$ |
| | | | | $DI_4$ | $Y_5$ | $Y_{13}$ | $Y_{21}$ | ... | $Y_{221}$ | $Y_{229}$ | $Y_{237}$ |
| | | | | $DI_5$ | $Y_6$ | $Y_{14}$ | $Y_{22}$ | ... | $Y_{222}$ | $Y_{230}$ | $Y_{238}$ |
| | | | | $DI_6$ | $Y_7$ | $Y_{15}$ | $Y_{23}$ | ... | $Y_{223}$ | $Y_{231}$ | $Y_{239}$ |
| | | | | $DI_7$ | $Y_8$ | $Y_{16}$ | $Y_{24}$ | ... | $Y_{224}$ | $Y_{232}$ | $Y_{240}$ |
| L | H | Input | Output | $DI_0$ | $Y_{240}$ | $Y_{232}$ | $Y_{224}$ | ... | $Y_{24}$ | $Y_{16}$ | $Y_8$ |
| | | | | $DI_1$ | $Y_{239}$ | $Y_{231}$ | $Y_{223}$ | ... | $Y_{23}$ | $Y_{15}$ | $Y_7$ |
| | | | | $DI_2$ | $Y_{238}$ | $Y_{230}$ | $Y_{222}$ | ... | $Y_{22}$ | $Y_{14}$ | $Y_6$ |
| | | | | $DI_3$ | $Y_{237}$ | $Y_{229}$ | $Y_{221}$ | ... | $Y_{21}$ | $Y_{13}$ | $Y_5$ |
| | | | | $DI_4$ | $Y_{236}$ | $Y_{228}$ | $Y_{220}$ | ... | $Y_{20}$ | $Y_{12}$ | $Y_4$ |
| | | | | $DI_5$ | $Y_{235}$ | $Y_{227}$ | $Y_{219}$ | ... | $Y_{19}$ | $Y_{11}$ | $Y_3$ |
| | | | | $DI_6$ | $Y_{234}$ | $Y_{226}$ | $Y_{218}$ | ... | $Y_{18}$ | $Y_{10}$ | $Y_2$ |
| | | | | $DI_7$ | $Y_{233}$ | $Y_{225}$ | $Y_{217}$ | ... | $Y_{17}$ | $Y_9$ | $Y_1$ |

(b) 16-bit Parallel Input Mode

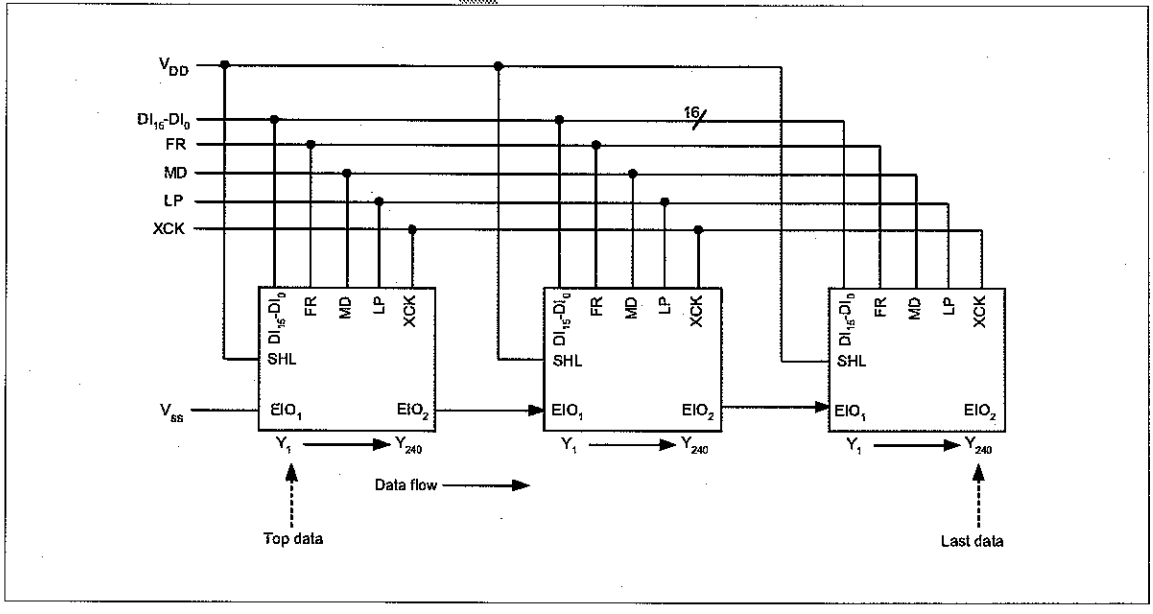
| MD | SHL | $EIO_1$ | $EIO_2$ | DATA INPUT | NUMBER OF CLOCKS | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 15 CLOCK | 14 CLOCK | 13 CLOCK | ... | 3 CLOCK | 2 CLOCK | 1 CLOCK |
| H | L | Output | Input | $DI_0$ | $Y_1$ | $Y_{17}$ | $Y_{33}$ | ... | $Y_{193}$ | $Y_{209}$ | $Y_{225}$ |
| | | | | $DI_1$ | $Y_2$ | $Y_{18}$ | $Y_{34}$ | ... | $Y_{194}$ | $Y_{210}$ | $Y_{226}$ |
| | | | | $DI_2$ | $Y_3$ | $Y_{19}$ | $Y_{35}$ | ... | $Y_{195}$ | $Y_{211}$ | $Y_{227}$ |
| | | | | $DI_3$ | $Y_4$ | $Y_{20}$ | $Y_{36}$ | ... | $Y_{196}$ | $Y_{212}$ | $Y_{228}$ |
| | | | | $DI_4$ | $Y_5$ | $Y_{21}$ | $Y_{37}$ | ... | $Y_{197}$ | $Y_{213}$ | $Y_{229}$ |
| | | | | $DI_5$ | $Y_6$ | $Y_{22}$ | $Y_{38}$ | ... | $Y_{198}$ | $Y_{214}$ | $Y_{230}$ |
| | | | | $DI_6$ | $Y_7$ | $Y_{23}$ | $Y_{39}$ | ... | $Y_{199}$ | $Y_{215}$ | $Y_{231}$ |
| | | | | $DI_7$ | $Y_8$ | $Y_{24}$ | $Y_{40}$ | ... | $Y_{200}$ | $Y_{216}$ | $Y_{232}$ |
| | | | | $DI_8$ | $Y_9$ | $Y_{25}$ | $Y_{41}$ | ... | $Y_{201}$ | $Y_{217}$ | $Y_{233}$ |
| | | | | $DI_9$ | $Y_{10}$ | $Y_{26}$ | $Y_{42}$ | ... | $Y_{202}$ | $Y_{218}$ | $Y_{234}$ |
| | | | | $DI_{10}$ | $Y_{11}$ | $Y_{27}$ | $Y_{43}$ | ... | $Y_{203}$ | $Y_{219}$ | $Y_{235}$ |
| | | | | $DI_{11}$ | $Y_{12}$ | $Y_{28}$ | $Y_{44}$ | ... | $Y_{204}$ | $Y_{220}$ | $Y_{236}$ |
| | | | | $DI_{12}$ | $Y_{13}$ | $Y_{29}$ | $Y_{45}$ | ... | $Y_{205}$ | $Y_{221}$ | $Y_{237}$ |
| | | | | $DI_{13}$ | $Y_{14}$ | $Y_{30}$ | $Y_{46}$ | ... | $Y_{206}$ | $Y_{222}$ | $Y_{238}$ |
| | | | | $DI_{14}$ | $Y_{15}$ | $Y_{31}$ | $Y_{47}$ | ... | $Y_{207}$ | $Y_{223}$ | $Y_{239}$ |
| | | | | $DI_{15}$ | $Y_{16}$ | $Y_{32}$ | $Y_{48}$ | ... | $Y_{208}$ | $Y_{224}$ | $Y_{240}$ |
| H | H | Input | Output | $DI_0$ | $Y_{240}$ | $Y_{224}$ | $Y_{208}$ | ... | $Y_{48}$ | $Y_{32}$ | $Y_{16}$ |
| | | | | $DI_1$ | $Y_{239}$ | $Y_{223}$ | $Y_{207}$ | ... | $Y_{47}$ | $Y_{31}$ | $Y_{15}$ |
| | | | | $DI_2$ | $Y_{238}$ | $Y_{222}$ | $Y_{206}$ | ... | $Y_{46}$ | $Y_{30}$ | $Y_{14}$ |
| | | | | $DI_3$ | $Y_{237}$ | $Y_{221}$ | $Y_{205}$ | ... | $Y_{45}$ | $Y_{29}$ | $Y_{13}$ |
| | | | | $DI_4$ | $Y_{236}$ | $Y_{220}$ | $Y_{204}$ | ... | $Y_{44}$ | $Y_{28}$ | $Y_{12}$ |
| | | | | $DI_5$ | $Y_{235}$ | $Y_{219}$ | $Y_{203}$ | ... | $Y_{43}$ | $Y_{27}$ | $Y_{11}$ |
| | | | | $DI_6$ | $Y_{234}$ | $Y_{218}$ | $Y_{202}$ | ... | $Y_{42}$ | $Y_{26}$ | $Y_{10}$ |
| | | | | $DI_7$ | $Y_{233}$ | $Y_{217}$ | $Y_{201}$ | ... | $Y_{41}$ | $Y_{25}$ | $Y_9$ |
| | | | | $DI_8$ | $Y_{232}$ | $Y_{216}$ | $Y_{200}$ | ... | $Y_{40}$ | $Y_{24}$ | $Y_8$ |
| | | | | $DI_9$ | $Y_{231}$ | $Y_{215}$ | $Y_{199}$ | ... | $Y_{39}$ | $Y_{23}$ | $Y_7$ |
| | | | | $DI_{10}$ | $Y_{230}$ | $Y_{214}$ | $Y_{198}$ | ... | $Y_{38}$ | $Y_{22}$ | $Y_6$ |
| | | | | $DI_{11}$ | $Y_{229}$ | $Y_{213}$ | $Y_{197}$ | ... | $Y_{37}$ | $Y_{21}$ | $Y_5$ |
| | | | | $DI_{12}$ | $Y_{228}$ | $Y_{212}$ | $Y_{196}$ | ... | $Y_{36}$ | $Y_{20}$ | $Y_4$ |
| | | | | $DI_{13}$ | $Y_{227}$ | $Y_{211}$ | $Y_{195}$ | ... | $Y_{35}$ | $Y_{19}$ | $Y_3$ |
| | | | | $DI_{14}$ | $Y_{226}$ | $Y_{210}$ | $Y_{194}$ | ... | $Y_{34}$ | $Y_{18}$ | $Y_2$ |
| | | | | $DI_{15}$ | $Y_{225}$ | $Y_{209}$ | $Y_{193}$ | ... | $Y_{33}$ | $Y_{17}$ | $Y_1$ |

## CONNECTION EXAMPLES OF MULTIPLE SEGMENT DRIVERS

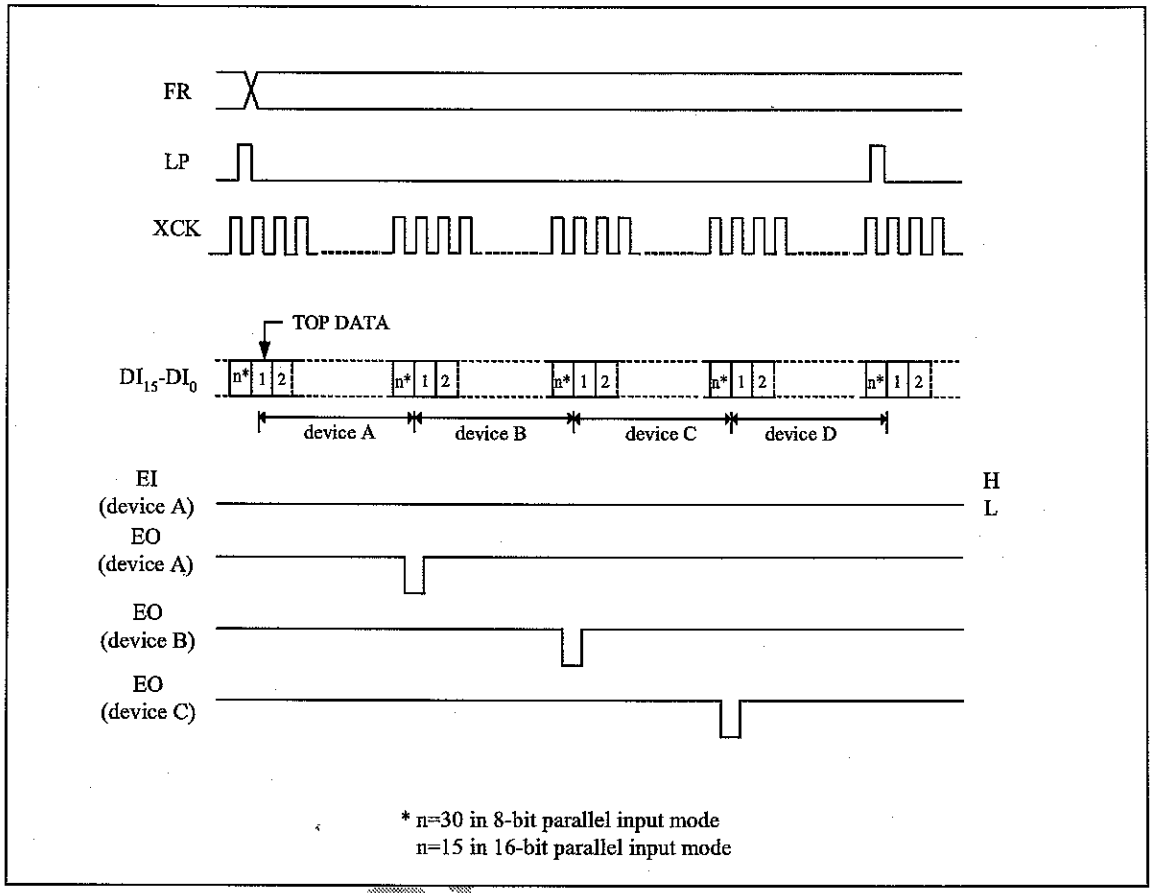
### (a) When SHL= "L"




### (b) When SHL= "H"



## TIMING CHART OF 4-DEVICE CASCADE CONNECTION OF SEGMENT DRIVERS




* n=30 in 8-bit parallel input mode
n=15 in 16-bit parallel input mode

**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER | SYMBOL | APPLICABLE PINS | RATING | UNIT | NOTE |
|---|---|---|---|---|---|
| Supply voltage (1) | $V_{DD}$ | $V_{DD}$ | -0.3 to +7.0 | V | 1,2 |
| Supply voltage (2) | $V_0$ | $V_{0L}$, $V_{0R}$ | -0.3 to +45.0 | V | |
| | $V_{12}$ | $V_{12L}$, $V_{12R}$ | -0.3 to V0 +0.3 | V | |
| | $V_{34}$ | $V_{34L}$, $V_{34R}$ | -0.3 to V0 +0.3 | V | |
| | $V_5$ | $V_{5L}$, $V_{5R}$ | -0.3 to V0 +0.3 | V | |
| Input voltage | $V_I$ | $DI_0$-$DI_{15}$, XCK, LP, FR, MD, SHL, $EIO_1$, $EIO_2$, /DISPOFF | -0.3 to VDD +0.3 | V | |
| Storage temperature | $T_{STG}$ | | -45 to +125 | ℃ | |

**NOTES**

1. TA= +25 ℃
2. The maximum applicable voltage on any pin with respect to $V_{SS}$ (0 V).

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Supply voltage (1) | $V_{DD}$ | $V_{DD}$ | +2.5 | | +5.5 | V | 1,2 |
| Supply voltage (2) | $V_0$ | $V_{0L}$, $V_{0R}$ | +10.0 | | +42.0 | V | |
| Operating temperature | $T_{OPR}$ | | -20 | | +85 | ℃ | |

**NOTES:**

1. The applicable voltage on any pin with respect to $V_{SS}$ (0 V).
2. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{34} < V_{12} < V_0$.

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{SS}$ = $V_5$ = 0 V, $V_{DD}$ = +2.5 to +5.5 V, $V_0$ = +10.0 to +42.0 V, $T_{OPR}$ = -20 to +85 ℃)

| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | $DI_{15}$-$DI_0$, XCK, LP, SHL, FR, MD, $EIO_1$, $EIO_2$, /DISPOFF | | | $0.3V_{DD}$ | V | |
| Input "High" voltage | $V_{IH}$ | | | $0.7V_{DD}$ | | | V | |
| Output "Low" voltage | $V_{OL}$ | $I_{OL}$=+0.4 mA | $EIO_1$, $EIO_2$ | | | +0.4 | V | |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$=-0.4 mA | | $V_{DD}$-0.4 | | | V | |
| Input leakage current | $I_{LI}$ | $V_{SS}$ <= $V_{IN}$ <= $V_{DD}$ | All input pins | | | +/-10.0 | μA | |
| I/O leakage current | $I_{LI/O}$ | $V_{SS}$ <= $V_{IN}$ <= $V_{DD}$ | $EIO_1$, $EIO_2$ | | | +/-10.0 | μA | |
| Output resistance | $R_{ON}$ | $\lvert\Delta V_{ON}\rvert$ =0.5V, $V_0$=40V | $Y_1$-$Y_{240}$ | | 0.8 | 1.3 | KΩ | |
| | | $\lvert\Delta V_{ON}\rvert$ =0.5V, $V_0$=30V | | | 1.3 | 1.8 | | |
| | | $\lvert\Delta V_{ON}\rvert$ =0.5V, $V_0$=20V | | | 1.8 | 2.3 | | |
| Standby current | $I_{STB}$ | | $V_{SS}$ | | | 75.0 | μA | 1 |
| Supply current (1) (Non-active Mode) | $I_{DD1}$ | | $V_{DD}$ | | | 2.4 | mA | 2 |
| Supply current (2) (Active Mode) | $I_{DD2}$ | | $V_{DD}$ | | | 14.4 | mA | 3 |
| Supply current (3) | $I_0$ | | $V_{0L}$, $V_{0R}$ | | | 2.0 | mA | 4 |

**NOTES:**

1. $V_{DD}$ = +5.0 V, $V_0$ = +40.0 V, $V_{IH}$ = $V_{DD}$, $V_{IL}$ = $V_{SS}$.
2. $V_{DD}$ = +5.0 V, $V_0$ = +40.0 V, $f_{XCK}$ = 25 MHz, no-load,
   EI = $V_{DD}$.
   The input data is turned over by data taking clock (16-bit parallel input mode).
3. $V_{DD}$ = +5.0 V, $V_0$ = +40.0 V, $f_{XCK}$ = 25 MHz, no-load,
   EI = $V_{SS}$.
   The input data is turned over by data taking clock (16-bit parallel input mode).
4. $V_{DD}$ = +5.0 V, $V_0$ = +40.0 V, $f_{XCK}$ = 25 MHz,
   $f_{LP}$ = 38.4 kHz, $f_{FR}$ = 80 Hz, no-load.
   The input data is turned over by data taking clock (16-bit parallel input mode).

**AC Characteristics**

(Mode 1) ($V_{SS}$ = $V_5$ = 0 V, $V_{DD}$ = +5.0 to ±0.5 V, $V_0$ = +10.0 to +42.0 V, $T_{OPR}$ = -20 to +85 ℃)

(the figure in parenthesis applies when $T_{OPR1}$ = -20 to +60 ℃)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Shift clock period | $t_{WCK}$ | $t_R$, $t_F$≤ 7 (5) ns | 40(36) | | | ns | 1 |
| Shift clock "H" pulse width | $t_{WCKH}$ | | 12 | | | ns | |
| Shift clock "L" pulse width | $t_{WCKL}$ | | 14 | | | ns | |
| Data setup time | $t_{DS}$ | | 5 | | | ns | |
| Data hold time | $t_{DH}$ | | 15 | | | ns | |
| Latch pulse "H" pulse width | $t_{WLPH}$ | | 15 | | | ns | |
| Shift clock rise to latch pulse rise time | $t_{LD}$ | | 5 | | | ns | |
| Shift clock fall to latch pulse fall time | $t_{SL}$ | | 25 | | | ns | |
| Latch pulse rise to shift clock rise time | $t_{LS}$ | | 25 | | | ns | |
| Latch pulse fall to shift clock fall time | $t_{LH}$ | | 25 | | | ns | |
| Enable setup time | $t_S$ | | 5(4) | | | ns | |
| Input signal rise time | $t_R$ | | | | 50 | ns | 2 |
| Input signal fall time | $t_F$ | | | | 50 | ns | 2 |
| Output delay time (1) | $t_D$ | $C_L$= 15 pF | | | 28(27) | ns | |
| Output delay time (2) | $t_{PD1}$ | $C_L$= 15 pF | | | 1.2 | µs | |
| Output delay time (3) | $t_{PD2}$ | $C_L$= 15 pF | | | 1.2 | µs | |

**NOTES:**

1. Takes the cascade connection into consideration.
2. ($t_{WCK}$- $t_{WCKH}$- $t_{WCKL}$)/2 is maximum in the case of high speed operation.

(Mode 2) ($V_{SS}$ = $V_5$ = 0 V, $V_{DD}$ = +3.0 to +4.5 V, $V_0$ = +10.0 to +42.0 V, $T_{OPR}$ = -20 to +85 ℃)

(the figure in parenthesis applies when $T_{OPR1}$ = -20 to +60 ℃)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Shift clock period | $t_{WCK}$ | $t_R$, $t_F$≤ 10 ns | 66(60) | | | ns | 1 |
| Shift clock "H" pulse width | $t_{WCKH}$ | | 23(20) | | | ns | |
| Shift clock "L" pulse width | $t_{WCKL}$ | | 23(20) | | | ns | |
| Data setup time | $t_{DS}$ | | 10 | | | ns | |
| Data hold time | $t_{DH}$ | | 25(20) | | | ns | |
| Latch pulse "H" pulse width | $t_{WLPH}$ | | 30 | | | ns | |
| Shift clock rise to latch pulse rise time | $t_{LD}$ | | 10 | | | ns | |
| Shift clock fall to latch pulse fall time | $t_{SL}$ | | 30 | | | ns | |
| Latch pulse rise to shift clock rise time | $t_{LS}$ | | 30 | | | ns | |
| Latch pulse fall to shift clock fall time | $t_{LH}$ | | 30 | | | ns | |
| Enable setup time | $t_S$ | | 12(10) | | | ns | |
| Input signal rise time | $t_R$ | | | | 50 | ns | 2 |
| Input signal fall time | $t_F$ | | | | 50 | ns | 2 |
| Output delay time (1) | $t_D$ | $C_L$= 15 pF | | | 44(40) | ns | |
| Output delay time (2) | $t_{PD1}$ | $C_L$= 15 pF | | | 1.2 | µs | |
| Output delay time (3) | $t_{PD2}$ | $C_L$= 15 pF | | | 1.2 | µs | |

**NOTES:**

3. Takes the cascade connection into consideration.

4. ($t_{WCK}$- $t_{WCKH}$- $t_{WCKL}$)/2 is maximum in the case of high speed operation.

(Mode 3) ($V_{SS}$ = $V_5$ = 0 V, $V_{DD}$ = +2.5 to +3.0 V, $V_0$ = +10.0 to +42.0 V, $T_{OPR}$ = -20 to +85 ℃)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Shift clock period | $t_{WCK}$ | $t_R$, $t_F$≤ 10 ns | 82 | | | ns | 1 |
| Shift clock "H" pulse width | $t_{WCKH}$ | | 28 | | | ns | |
| Shift clock "L" pulse width | $t_{WCKL}$ | | 28 | | | ns | |
| Data setup time | $t_{DS}$ | | 10 | | | ns | |
| Data hold time | $t_{DH}$ | | 30 | | | ns | |
| Latch pulse "H" pulse width | $t_{WLPH}$ | | 30 | | | ns | |
| Shift clock rise to latch pulse rise time | $t_{LD}$ | | 10 | | | ns | |
| Shift clock fall to latch pulse fall time | $t_{SL}$ | | 30 | | | ns | |
| Latch pulse rise to shift clock rise time | $t_{LS}$ | | 30 | | | ns | |
| Latch pulse fall to shift clock fall time | $t_{LH}$ | | 30 | | | ns | |
| Enable setup time | $t_S$ | | 15 | | | ns | |
| Input signal rise time | $t_R$ | | | | 50 | ns | 2 |
| Input signal fall time | $t_F$ | | | | 50 | ns | 2 |
| Output delay time (1) | $t_D$ | $C_L$= 15 pF | | | 57 | ns | |
| Output delay time (2) | $t_{PD1}$ | $C_L$= 15 pF | | | 1.2 | µs | |
| Output delay time (3) | $t_{PD2}$ | $C_L$= 15 pF | | | 1.2 | µs | |

**NOTES:**

5. Takes the cascade connection into consideration.

6. ($t_{WCK}$- $t_{WCKH}$- $t_{WCKL}$)/2 is maximum in the case of high speed operation.

**Timing Chart of Segment Mode**

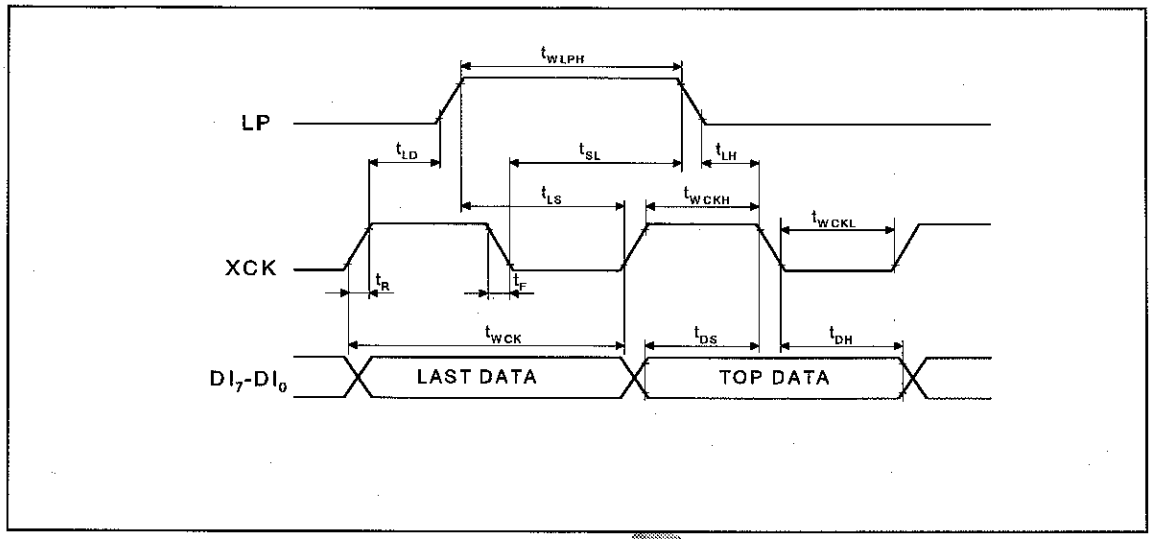



**Fig.6 Timing Characteristics (1)**

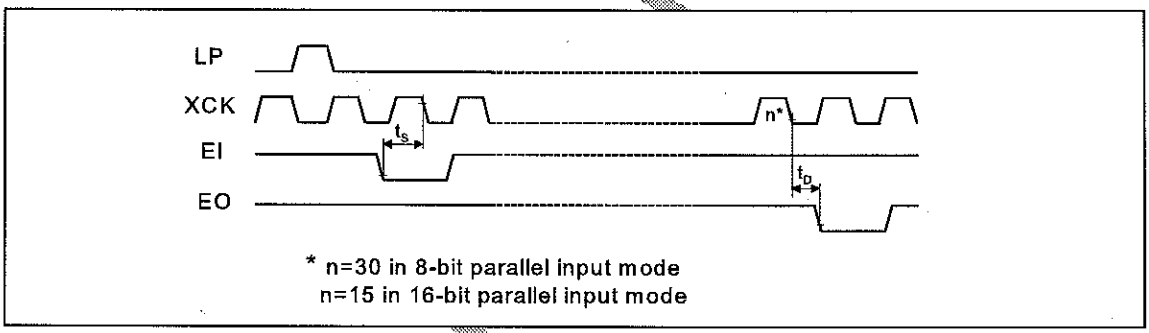



**Fig.7 Timing Characteristics (2)**

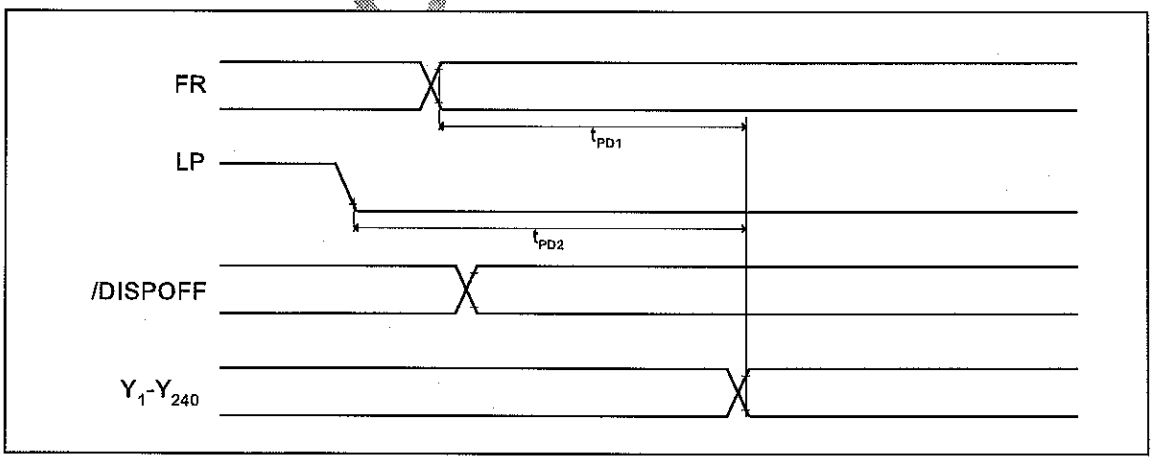



**Fig.8 Timing Characteristics (3)**

## PRECAUTIONS

**Precautions when connecting or disconnecting the power supply**

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω ) or fuse to the LCD drive power $V_0$ of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level $V_5$ on /DISPOFF function. Then, disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.